WHAT IS CLAIMED IS:

1. A method of data transmission, said method comprising:

receiving a first set of input signals and a second set of input signals, each input signal having a series of state transitions synchronized to a data clock signal having a period T_CLK;

transmitting corresponding first and second sets of output signals such that each output signal (1) corresponds to an input signal of the corresponding set, (2) passes along a corresponding one of a corresponding set of a plurality of conductive paths, and (3) has a series of state transitions corresponding to the series of state transitions of the corresponding input signal;

transmitting each among a third set of output signals on a corresponding one of a third set of the plurality of conductive paths; and

transmitting each among a fourth set of output signals on a corresponding one of a fourth set of the plurality of conductive paths,

wherein adjacent conductive paths of the first set are separated by at least one conductive path of the third set, and

wherein adjacent conductive paths of the second set are separated by at least one conductive path of the fourth set, and

wherein a time between a state transition on an input signal of the first set and the corresponding state transition on the corresponding output signal exceeds a time between a state transition on an input signal of the second set and the corresponding state transition on the corresponding output signal by a delay period T_DLY, and

wherein the period T_CLK is greater than the delay period T_DLY, and

wherein a first of two ends of each one among the plurality of conductive paths is closer to the first end of an adjacent conductive path than to the second end of the adjacent conductive path, and

wherein said transmitting each among the first and second sets of signals includes applying the signal to the first end of the corresponding conductive path, and wherein said transmitting each among the third and fourth sets of signals includes applying the signal to the second end of the corresponding conductive path.

2. The method of data transmission according to claim 1, wherein adjacent conductive paths of the first set are separated by at least one conductive path of the second set.

3. The method of data transmission according to claim 1, wherein the conductive paths of the plurality of conductive paths are substantially parallel to one another.

4. The method of data transmission according to claim 1, wherein transmitting each among a first, second, third, and fourth set of output signals occurs on the same semiconductor substrate.

5. The method of data transmission according to claim 4, wherein a length of each of the plurality of conductive paths is at least five centimeters.

6. The method of data transmission according to claim 1, said method further comprising transmitting a clock signal across one of the plurality of conductive paths, and

wherein each among the first set of output signals includes a series of state transitions synchronized to the clock signal.

7. The method of data transmission according to claim 1, wherein at least one among the first set of the plurality of conductive paths includes a first alternating sequence of inversions and regenerations, and

wherein at least one among the second set of the plurality of conductive paths includes a second alternating sequence of inversions and regenerations, said second sequence being opposite to the first sequence.

8. A method of data transmission, said method comprising:

transmitting each among a first set of signals on a corresponding one of a first set of a plurality of conductive paths;

transmitting each among a second set of signals on a corresponding one of a second set of the plurality of conductive paths;

transmitting each among a third set of signals on a corresponding one of a third set of the plurality of conductive paths; and

transmitting each among a fourth set of signals on a corresponding one of a fourth set of the plurality of conductive paths,

wherein adjacent conductive paths of the first set are separated by at least one conductive path of the third set, and

wherein adjacent conductive paths of the second set are separated by at least one conductive path of the fourth set, and

wherein a first of two ends of each one among the plurality of conductive paths is closer to the first end of an adjacent conductive path than to the second end of the adjacent conductive path, and

wherein said transmitting each among the first and second sets of signals includes applying the signal to the first end of the corresponding conductive path, and wherein said transmitting each among the third and fourth sets of signals includes applying the signal to the second end of the corresponding conductive path, and

wherein at least one among the first set of conductive paths includes a first alternating sequence of inversions and regenerations, and

wherein at least one among the second set of conductive paths includes a second alternating sequence of inversions and regenerations, said second sequence being opposite to the first sequence.

9. The method of data transmission according to claim 8, wherein the conductive paths of the plurality of conductive paths are substantially parallel to one another.

10. The method of data transmission according to claim 8, wherein adjacent conductive paths of the first set are separated by at least one conductive path of the second set.

11. The method of data transmission according to claim 8, wherein transmitting each among a first, second, third, and fourth set of output signals occurs on the same semiconductor substrate.

12. The method of data transmission according to claim 11, wherein a length of each of the plurality of conductive paths is at least five centimeters.

13. The method of data transmission according to claim 8, said method further comprising transmitting a clock signal across one of the plurality of conductive paths, and

wherein each among the first set of output signals includes a series of state transitions synchronized to the clock signal.

14. A method of data transmission, said method comprising:

receiving a first set of input signals and a second set of input signals, each input signal having a series of state transitions synchronized to a data clock signal having a period T_CLK; and

transmitting corresponding first and second sets of output signals such that each output signal (1) corresponds to an input signal of the corresponding set, (2) passes along a corresponding one of a corresponding set of a plurality of conductive paths, and (3) has a series of state transitions corresponding to the series of state transitions of the corresponding input signal,

wherein a time between a state transition on an input signal of the first set and the corresponding state transition on the corresponding output signal

exceeds a time between a state transition on an input signal of the second set and the corresponding state transition on the corresponding output signal by a delay period T_DLY, and

wherein the period T_CLK is greater than the delay period T_DLY, and

wherein adjacent conductive paths that each carry an output signal of the first set are separated by at least one conductive path that carries an output signal of the second set, and

wherein at least one among the first set of conductive paths includes a first alternating sequence of inversions and regenerations, and

wherein at least one among the second set of conductive paths includes a second alternating sequence of inversions and regenerations, said second sequence being opposite to the first sequence.

15. The method of data transmission according to claim 14, wherein the conductive paths of the plurality of conductive paths are substantially parallel to one another.

16. The method of data transmission according to claim 14, wherein transmitting each among the first and second sets of output signals occurs on the same semiconductor substrate.

17. The method of data transmission according to claim 16, wherein a length of each of the plurality of conductive paths is at least five centimeters.

18. The method of data transmission according to claim 14, said method further comprising transmitting a clock signal across one of the plurality of conductive paths, and

wherein each among the first set of output signals includes a series of state transitions synchronized to the clock signal.

19. A system for data transmission, said system comprising:

a plurality of conductive paths;

a first transmitter configured and arranged to receive a first set of input signals and a second set of input signals and to transmit corresponding first and second sets of output signals; and

a second transmitter configured and arranged to receive a third set of input signals and a fourth set of input signals and to transmit corresponding third and fourth sets of output signals,

wherein each input signal has a series of state transitions and each output signal has a series of state transitions corresponding to the series of state transitions of the corresponding input signal, and

wherein a first of two ends of each one among the plurality of conductive paths is closer to the first end of an adjacent conductive path than to the second end of the adjacent conductive path, and

wherein the first transmitter is further configured and arranged to apply each first output signal to the first end of a corresponding one of a first set of the plurality of conductive paths and to apply each second output signal to the

first end of a corresponding one of a second set of the plurality of conductive paths, and

wherein the second transmitter is further configured and arranged to apply each third output signal to the second end of a corresponding one of a third set of the plurality of conductive paths and to apply each fourth output signal to the second end of a corresponding one of a fourth set of the plurality of conductive paths, and

wherein adjacent conductive paths carrying output signals of the first set are separated by at least one conductive path carrying an output signal of the third set, and

wherein each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission lines, and

wherein at least one among the first set of the plurality of parallel transmission lines includes a first alternating series of inverting and non-inverting buffers, and

wherein at least one among the second set of the plurality of conductive paths includes a second alternating series of inverting and non-inverting buffers, and

wherein the sequence of inverting and non-inverting buffers in the second alternating series is opposite to the sequence of inverting and non-inverting buffers in the first alternating series.

20. The system for data transmission according to claim 19, wherein the conductive paths of the plurality of conductive paths are substantially parallel to one another.

21. The system for data transmission according to claim 19, wherein the first and second transmitters are fabricated on the same semiconductor substrate.

22. The system for data transmission according to claim 21, wherein a length of each of the conductive paths is at least five centimeters.

23. The system for data transmission according to claim 19, wherein each of the first and second transmitters is further configured and arranged to receive an operating voltage from two power rails, and

wherein the two power rails are parallel to and on opposite sides of the plurality of conductive paths.

24. The system for data transmission according to claim 19, wherein the first transmitter is further configured and arranged to couple a clock signal to one of the plurality of parallel transmission lines, and

wherein each among the first set of output signals includes a series of state transitions synchronized to the clock signal.

25. A system for data transmission, said system including:

a plurality of conductive paths; and

a data transmitter configured and arranged to receive a plurality of input signals, each having a series of state transitions synchronized to a data

clock signal having a period T_CLK, and to transmit a plurality of first output signals and a plurality of second output signals,

wherein each of the first and second output signals corresponds to a different one of the input signals and has a series of state transitions corresponding to the series of state transitions of the corresponding input signal, and

wherein the data transmitter is further configured and arranged to transmit each of the first and second output signals along a corresponding one of a corresponding set of the plurality of conductive paths, and

wherein a time between a state transition on an input signal and a corresponding state transition on a corresponding second output signal exceeds a time between a state transition on an input signal and a corresponding state transition on a corresponding first output signal by a delay period T_DLY, and

wherein the time period T_CLK is greater than the delay period T_DLY, and

wherein adjacent conductive paths of the first set are separated by a conductive path of the second set, and

wherein each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission lines, and

wherein at least one among the first set of the plurality of parallel transmission lines includes a first alternating series of inverting and non-inverting buffers, and

wherein at least one among the second set of the plurality of conductive paths includes a second alternating series of inverting and non-inverting buffers, and

wherein the sequence of inverting and non-inverting buffers in the second alternating series is opposite to the sequence of inverting and non-inverting buffers in the first alternating series.

26. The system for data transmission according to claim 25, wherein the conductive paths of the plurality of conductive paths are substantially parallel to one another.

27. The system for data transmission according to claim 25, wherein the first and second transmitters are fabricated on the same semiconductor substrate.

28. The system for data transmission according to claim 27, wherein a length of each of the conductive paths is at least five centimeters.

29. The system for data transmission according to claim 25, wherein each of the first and second transmitters is further configured and arranged to receive an operating voltage from two power rails, and

wherein the two power rails are parallel to and on opposite sides of the plurality of conductive paths.

30. The system for data transmission according to claim 25, wherein the first transmitter is further configured and arranged to couple a clock signal to one of the plurality of parallel transmission lines, and

wherein each among the first set of output signals includes a series of state transitions synchronized to the clock signal.

31. The system for data transmission according to claim 25, wherein the delay period T_DLY is at least twice as long as a rise time of the data clock signal.

32. A system for data transmission, said system including:

a plurality of conductive paths; and

a first data transmitter configured and arranged to receive a plurality of input signals, each having a series of state transitions synchronized to a data clock signal having a period T_CLK, and to transmit a plurality of first output signals and a plurality of second output signals; and

a second data transmitter configured and arranged to receive a plurality of input signals, each having a series of state transitions synchronized to a data clock signal, and to transmit a plurality of third output signals and a plurality of fourth output signals,

wherein each of the first, second, third, and fourth output signals corresponds to a different one of the input signals and has a series of state transitions corresponding to the series of state transitions of the corresponding input signal, and

wherein the first and second data transmitters are further configured and arranged to transmit each of the first, second, third, and fourth output signals along a corresponding one of a corresponding set of the plurality of conductive paths, and

wherein a time between a state transition on an input signal and a corresponding state transition on a corresponding second output signal exceeds a time between a state transition on an input signal and a corresponding state transition on a corresponding first output signal by a delay period T_DLY, and

wherein the time period T_CLK is greater than the delay period T_DLY, and

wherein adjacent conductive paths of the first set are separated by a conductive path of the third set, and

wherein a first of two ends of each one among the plurality of conductive paths is closer to the first end of an adjacent conductive path than to the second end of the adjacent conductive path, and

wherein the first data transmitter is configured and arranged to apply each first and second output signal to the first end of the corresponding conductive path, and

wherein the second data transmitter is configured and arranged to apply each third and fourth output signal to the second end of the corresponding conductive path.

33. The system for data transmission according to claim 32, wherein the first and second transmitters are fabricated on the same semiconductor substrate.

34. The system for data transmission according to claim 33, wherein a length of each of the conductive paths is at least five centimeters.

35. The system for data transmission according to claim 32, wherein each of the first and second transmitters is further configured and arranged to receive an operating voltage from two power rails, and

wherein the two power rails are parallel to and on opposite sides of the plurality of conductive paths.

36. The system for data transmission according to claim 32, wherein each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission lines, and

wherein the first transmitter is further configured and arranged to couple a clock signal to one of the plurality of parallel transmission lines, and

wherein each among the first set of output signals includes a series of state transitions synchronized to the clock signal.

37. The system for data transmission according to claim 32, wherein each one among the plurality of conductive paths includes a corresponding one of a plurality of transmission lines, and

wherein at least one among the first set of the plurality of parallel transmission lines includes a first alternating series of inverting and non-inverting buffers, and

wherein at least one among the second set of the plurality of conductive paths includes a second alternating series of inverting and non-inverting buffers, and

wherein the sequence of inverting and non-inverting buffers in the second alternating series is opposite to the sequence of inverting and non-inverting buffers in the first alternating series.

38. A data transmitter configured and arranged to receive a plurality of input signals and to transmit a plurality of first output signals and a plurality of second output signals, each of the first and second output signals corresponding to a different one of the input signals and each being transmitted along a corresponding one of a corresponding set of the plurality of conductive paths, said data transmitter comprising:

a plurality of first latches, each having (1) a clock input configured and arranged to receive a first clock signal including a series of first transitions, with consecutive first transitions being separated by a time period T_CLK, (2) a latch input configured and arranged to receive a corresponding one of the input signals, and (3) an latch output configured and arranged to produce a corresponding latch signal, each first latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each first transition; and

a plurality of second latches, each having (1) a clock input configured and arranged to receive a second clock signal based on the first clock signal and including a series of second transitions, with consecutive second transitions being separated by a time period T_CLK, (2) a latch input configured and arranged to receive a corresponding input signal, and (3) a latch output configured and arranged to produce a corresponding latch signal, each second latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each second transition;

wherein each first output signal is based on a latch signal of a different one of the first latches and each second output signal is based on a latch signal of a different one of the second latches, and

wherein a time between a transition on an input signal and a corresponding transition on a corresponding second output signal exceeds a time between a transition on an input signal and a corresponding transition on a corresponding first output signal by a delay period T_DLY, and

wherein the time period T_CLK is greater than the delay period T_DLY, and

wherein adjacent conductive paths of the first set are separated by a conductive path of the second set, and

wherein each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission lines, and

wherein at least one among the first set of the plurality of parallel transmission lines includes a first alternating series of inverting and non-inverting buffers, and

wherein at least one among the second set of the plurality of conductive paths includes a second alternating series of inverting and non-inverting buffers, and

wherein the sequence of inverting and non-inverting buffers in the second alternating series is opposite to the sequence of inverting and non-inverting buffers in the first alternating series.

39. The data transmitter according to claim 38, wherein the conductive paths of the plurality of conductive paths are substantially parallel to one another.

40. The data transmitter according to claim 38, wherein the first and second transmitters are fabricated on the same semiconductor substrate.

41. The data transmitter according to claim 40, wherein a length of each of the conductive paths is at least five centimeters.

42. The data transmitter according to claim 38, said data transmitter further comprising two power rails,

wherein the data transmitter is further configured and arranged to receive an operating voltage from the two power rails, and

wherein the two power rails extend parallel and adjacent to, and on opposite sides of, the plurality of conductive paths.

43. The data transmitter according to claim 38, wherein the first transmitter is further configured and arranged to couple a clock signal to one of the plurality of parallel transmission lines, and

wherein each among the first set of output signals includes a series of state transitions synchronized to the clock signal.

44. The data transmitter according to claim 38, wherein the delay period T_DLY is at least twice as long as a rise time of the data clock signal.